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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/574,653	05/18/2000	Youngmin Kim	TI-29012	8503

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/574,653	KIM ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

8/18/2004

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Claims 1-3 and 9-12 are pending in the application. The 112-second-paragraph rejection to claim 1 is withdrawn.

2. The Final rejection, as set forth in the previous Office Action mailed on 4/21/2004, is withdrawn in response to the arguments submitted in the personal interview on 7/21/2004.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation " said etching of said initial single layer sidewall structure is an anisotropic etch ." There is insufficient antecedent basis in the originally filed specification for this limitation in the claim.

In originally filed specification, page 8, lines 2-9, it discloses that the additional sidewall etch for reducing the width of the NMOS sidewalls 110 is by "relatively isotropic", instead of "anisotropic etch", as claimed. The Examiner believes that the "anisotropic etch" as recited in claim 2 has been mixed up with the etch step for forming the "initial single layer sidewall structures" 101, in which the sidewalls 101 are formed by the anisotropic etching.

For the above reason, this Office Action is based on the best understanding of the Examiner.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Masuoka (US 5,994,743) in view of Wang et al. (US 6,020,231).

In re claims 1 and 3, Masuoka, in Figs. 2a-2g and related text, teaches the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- forming a PMOS transistor gate structure 30 on a n-type region 23 of a semiconductor substrate 21 (Fig.2a-2b);
- forming a NMOS transistor gate structure 29 on a p-type region 24 of said semiconductor substrate 21 (Fig.2a-2b);
- forming initial single layer sidewall structures 33, composed of *silicon oxide* (col. 6, lines 4-9), of similar widths adjacent to said NMOS gate structure 29 and said PMOS transistor gate structure 30 (Fig.2c);
- ion-implanting to form damage layer 39 on the sidewall structure adjacent to PMOS transistor gate structure 30 (Fig.2e); and
- etching said initial single layer sidewall structure 33 adjacent to said **PMOS** transistor gate structure 30 such that the width of a first single layer sidewall

structure adjacent to said **PMOS** transistor gate structure 30 is less than the width of a second single layer sidewall structure adjacent to said NMOS transistor gate structure 29 (Fig.2f).

Masuoka, in the preferred embodiment, teaches a method just opposite to what are recited in the instant invention. In other word, Masuoka teaches forming a narrower sidewall structure adjacent to PMOS transistor (Fig.2f),whereas the instant invention discloses forming a narrower sidewall structure adjacent to NMOS transistor.

Masuoka, however, suggests the **desirability** of **switching** the features of both NMOS and PMOS transistors **around** as desired. Particularly, Masuoka states that " the nMOSFET is formed of the LDD structure and the pMOSFET is formed of the single drain structure in the embodiments, **but** they may also be formed by the **other way around, respectively**." (col. 6, lines 50-53). (Emphasis added)

What Masuoka suggests above is that, in the preferred embodiments, the **narrower sidewall structure is associated with** the transistor having **single drain structure** as illustrated in Fig.2g, which happens to be the **PMOS** transistor. However, it can be formed the other way around, as suggested by Masuoka, such that the **narrower sidewall structure is associated with** the **NMOS** transistor having single drain structure, whereas the wider sidewall structure is associated with the PMOS transistor.

As such, one of the ordinary skill in the art would have been comprehend that having the narrower sidewall structure with NOMS it also means that the sidewall width adjacent to said NMOS transistor gate structure 30 is less than the sidewall width adjacent to said PMOS transistor gate structure 29, since a resultant structure can be obtained naturally as

the process is reconstructed at the other way around, as suggested by Masuoka at col. 6, lines 50-53.

In re claim 2, Masuoka teaches etching said initial single layer sidewall structure by wet etching (col. 6, lines 28-30), which is a relatively isotropic etching, which is same as the teaching in the originally filed specification.

In re claims 9, 10 and 12, Masuoka also teaches the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- providing a semiconductor substrate 21 of a first conductivity type (p-type, col. 5, line 43) with a region of a second conductivity type (n-type) region 23 (Fig.2a);
- forming a gate dielectric 25 on said semiconductor substrate 21 (Fig.2a);
- forming a conductive layer 26 on said gate dielectric 25 (Fig.2a);
- etching said conductive layer 26 and said gate dielectric 25 to form a first transistor gate stack 29 (i.e. NMOS) with an upper surface 24 on said semiconductor substrate of a first conductivity (p-type) and a second transistor gate stack 30 (i.e. PMOS) with an upper surface 23 on said region of said semiconductor substrate of a second conductivity type (n-type) (Fig.2a);
- forming a sidewall film (i.e. a conformal SiO2 film, col. 6, lines 4-9) over said semiconductor substrate 21;
- anisotropically etching said sidewall film (col. 6, lines 6-9) such that all of the sidewall film is removed from said upper surface of said first transistor gate stack (NMOS) and said upper surface of said second transistor gate stack (PMOS), wherein a plurality of sidewall structures 33 of a first width are

formed adjacent to said first (NMOS) and second (PMOS) transistor gate stacks (Fig.2c);

- masking said second transistor gate stack (PMOS) with a photoresist pattern 34 used for source/drain implantation 35 (Fig. 2d);
- ion-implanting to form damage layer 39 on the sidewall structure adjacent to PMOS transistor gate structure 30 (Fig.2e); and
- etching said sidewalls of said first width adjacent to said **second** transistor gate stack (PMOS) thereby forming sidewalls of a second width adjacent to said **second** transistor gate stack (PMOS), wherein said second width is **less** than said first width (Fig.2f).

Masuoka does not teach forming sidewalls of a second width adjacent to said first transistor gate stack (i.e. NMOS).

However, Masuoka's suggestion, as stated above, would remedy the above deficiency with a reasonable motivation, as stated previously.

In re claim 11, Masuoka substantially teach the claimed method as stated above but is silent as to utilizing plasma etch process in the anisotropically etching step.

However, the plasma etch is a well-known practice for etching a sidewall film to form the sidewalls of a CMOS device, as evidenced by Wang et al., in which they states that " a conventional fabrication technique for forming such side wall spacer is by way of CVD forming of an oxide layer, and a subsequent step of anisotropic etching, typically either reactive ion etching or plasma etching." (col. 1, lines 40-43).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention was made to use the plasma etch as taught by Wang et al. to

anisotropically etch the sidewall film of Masuoka for the purpose of forming sidewall structure of said PMOS and said NMOS transistors, since said plasma etch is a reliable method for selectively etching sidewall film with good dimension control. (col. 1, lines 40-43, Wang et al.).

Response to Arguments

7. Applicant's arguments filed 1/30/04 have been fully considered and are persuasive. Therefore, the final rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as in this Office Action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Primary Examiner
Art Unit 2823

August 18, 2004

HSIEN-MING LEE
PRIMARY EXAMINER